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EXAMINER	
FOSTER, P	
ART UNIT	**PAPER NUMBER**
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/115,444	Chen et al.
Examiner	**Group Art Unit**
David Foster	2841

☒ Responsive to communication(s) filed on *Jan 24, 2001* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-22* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-22* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *Jan 24, 2001* is ☒approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

HIGH DENSITY INTERNAL BALL GRID ARRAY INTEGRATED CIRCUIT PACKAGE

Chen et al.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "high density ball grid array" in claim 6 is a relative term which renders the claim indefinite. The term "high density ball grid array" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term high density ball grid array does not define the metes and bounds necessary to ascribe whether the ball grid array is high density or low density.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (5,886,876) and Ellerson et al. (5,669,137).

Reference claim 1 and 8. Yamaguchi discloses an integrated circuit package comprising: a substrate (Figure 2, item 11) having a plurality of peripheral openings (Figure 1, items 19) and first and second surfaces (Figure 2c); a chip adhered to said second surface of said substrate (Figure 2c, item 13); **a plurality of electrical conductors coupled to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate** (column 3, line 52); a plurality of pads disposed on said first surface of said substrate generally centralized within said peripheral openings of said substrate (Figure 2, items 14); and wire bonding electrically connecting said chip to said substrate between said bonding pads and said routing strips (Figure 2c, item 21 and column 4, line 36).. Yamaguchi does not disclose potting material filling said peripheral openings. Ellerson et al. disclose a protective encapsulant material (Figure 2, item 61). It would have been obvious at the time the invention was made to a person having

ordinary skill in the art to provide encapsulant as disclosed by Ellerson et al. with the Yamaguchi package.

Reference claim 2. Yamaguchi does not disclose a substrate having first and second layer. However, it should be understood by one skilled in the art that substrates may consist of a single layer or may be a multilayered board having an alternate nuymber of layers.

Reference claim 3. Yamaguchi discloses an integrated circuit package as recited in claim 1 further comprising a plurality of routing strips being integral with said substrate (Figure 2, items 14).

Reference claim 4. Yamaguchi discloses an integrated circuit package as recited in claim 3 wherein at least one of said pads disposed on said first surface of said substrate is electrically connected with at least one of said routing strips (Figure 2c, item 21).

Reference claim 5.Yamaguchi discloses an integrated circuit package as recited in claim 1 further comprising at least one solder ball disposed on one of said pads (Figure 2c, items 18).

Reference claim 6.Yamaguchi discloses an integrated circuit package as recited in claim 1 further comprising a plurality of solder balls (Figure 1, items 18) disposed on said pads forming a high density ball grid array.

Reference claim 7.Yamaguchi discloses an integrated circuit package as recited in claim 1 wherein said potting material adheres said chip to said substrate (Figure 2c and column 5, line 35).

Reference claim 9.Yamaguchi discloses an integrated circuit package as recited in claim 8 further comprising at least one solder ball disposed on one of said pads (Figure 1, item 18).

Reference claim 10. Yamaguchi **does not discloses** an integrated circuit package as recited in claim 9 wherein said at least one solder ball is between about 8 and 20 mils in diameter. However, even though Yamaguchi does not disclose the diameter of the solder balls, the scope of the Yamaguchi package is similar and the Yamaguchi package could, indeed, include solder balls which range in size from 8 to 20 mils in diameter.

Reference claim 11.Yamaguchi discloses an integrated circuit package as recited in claim 8 further comprising a plurality of solder balls disposed on said pads forming a high density ball grid array (Figure 2c, items 18).

Reference claim 12.Yamaguchi **does not discloses** an integrated circuit package as recited in claim, to 8 wherein said chip has a thickness between about 10 and 20 mils. However, even though Yamaguchi does not disclose the thickness of the chip, the scope of the Yamaguchi package is similar and the Yamaguchi package could, indeed, include chips which range in size from 10 to 20 mils in thickness.

Reference claim 13, 14 and 15.Yamaguchi **does not discloses** an integrated circuit package as recited in claim 8 wherein said substrates have a thicknesses of between about 8 and 28 mils. However, even though Yamaguchi does not disclose the thickness of the substrate, the scope of the Yamaguchi package is similar and the Yamaguchi package could, indeed, include a substrate which ranges in thickness from 8 to 28 mils in thickness.

Reference claim 16. Yamaguchi discloses an integrated circuit package comprising: a substrate having a plurality of peripheral openings (Figure 1, items 19), first and second surfaces (Figure 2c) and an outline; a plurality of routing strips being integral with said substrate (Figure 2c, items 14); a plurality of pads centrally disposed on said first surface at least one of said pads being electrically connected with said routing strips (Figure 2c, items 21); a chip adhered to said second surface of said substrate (Figure 2c, item 13), said chip having an outline that is substantially the same as said outline of said substrate (Figure 2a) and having a plurality of bonding pads (Figure 2a, items 14); wire bonding electrically connecting said bonding pads to said routing strips (Figure 2a, items 21); vias connecting said routing strips to said pads (Figure 2a, items 17); potting material filling said peripheral openings and covering said wire bonding and said bonding pads (Figure 6, item 25 and column 6, line 58); and a plurality of solder balls centrally disposed on said pads disposed on said first surface of said substrate forming a high density ball grid array (Figure 2c, items 18).

Reference claim 17, 18, 19 and 20.Yamaguchi **does not discloses** an integrated circuit package as recited in claim 16 wherein said chip has a thickness between about 10 and 20 mils, said substrate has a thickness of between about 8 and 28 mils, said substrate has first and second layers and therein said first layer has a thickness of about 12 mils and said second layer has a thickness of about 8 mils and said substrate has first, second and third layers and wherein said first layer has a thickness of about 12 mils. However, even though Yamaguchi does not disclose

the chip thickness, thickness of the substrate, the scope of the Yamaguchi package is similar and the Yamaguchi package could, indeed, include a substrate which ranges in thickness from 8 to 28 mils in thickness.

Reference claim 21, Yamaguchi discloses an integrated circuit package of claim 1 wherein each of the plurality of conductors comprises a bonding pad (Figure 6, item 25 and column 6, line 58).

Reference claim 22, Yamaguchi discloses an integrated package comprising:

a substrate (Figure 2, item 11) having a plurality of peripheral opening (Figure 1, items 19) and first and second surfaces (Figure 2c);

a chip comprising an operative side and a non-operative side (Figure 2), wherein said chip is adhered to said second surface of said substrate such that the non-operative side faces away from the substrate (Figure 2);

a plurality of pads disposed on said first surface of said substrate generally centralized within said peripheral openings of said substrate (Figure 2, items 14). **Yamaguchi does not disclose** potting material filling said peripheral openings. Ellerson et al. disclose a protective encapsulant material (Figure 2, item 61). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide encapsulant as disclosed by Ellerson et al. with the Yamaguchi package.

Conclusion

5. Any inquiry concerning to this communication or earlier communications from the Examiner should be directed to David Foster whose telephone number is (703) 308-1763. The examiner can normally be reached on Monday through Thursday and alternate Fridays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Jeffrey A. Gaffin, who can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703)308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DAF

March 16, 2001

Jayprakash N. Gandhi
Primary Examiner
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